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Review—Extremely Thin Amorphous Indium Oxide Transistors

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Amorphous oxide semiconductor transistors have been a mature technology in display panels for upward of a decade, and have recently been considered as promising back-end-of-line compatible channel materials for monolithic 3D applications. However, achieving high-mobility amorphous semiconductor materials with comparable performance to traditional crystalline semiconductors has been a long-standing problem. Recently it has been found that greatly reducing the thickness of indium oxide, enabled by an atomic layer deposition (ALD) process, can tune its material properties to achieve high mobility, high drive current, high on/off ratio, and enhancement-mode operation at the same time, beyond the capabilities of conventional oxide semiconductor materials. In this work, the history leading to the re-emergence of indium oxide, its fundamental material properties, growth techniques with a focus on ALD, state-of-the-art indium oxide device research, and the bias stability of the devices are reviewed.

1. Introduction

Indium oxide has historically proved troublesome to work within the context of electronic devices. The greatest difficulty is its uncontrollable degenerate carrier concentration—even in crystalline form with the most careful modern growth techniques it is very difficult to achieve a carrier concentration of less than 10^{17} cm^{-3}[1] Typical results are two to four orders of magnitude higher (particularly for disordered material), far too high to be modulated effectively by a traditional transistor's gate. After the development of the thin-film transistor (TFT) in the 1960's,[2] oxide semiconductor TFTs were quickly reported.[3–6] Functional devices with relatively high carrier mobilities were fabricated, however, in general, weak gate modulation was observed to the point where these materials were frequently classed as (transparent) conductors rather than semiconductors.[7] Ref. [3] in particular mentions using indium oxide as a channel material, but reports no transistor data. The reason is certainly degenerately high carrier concentration. The relatively weak performance of oxide semiconductor devices, particularly in contrast with the immense success of silicon which was rapidly being commercialized at that time,[8] had a cooling effect on research efforts after the initial reports.

A second, subtler issue that will be important for the following discussion is the strong tendency of indium oxide to crystallize, shared in common with many of the binary metal oxides. Amorphous material is highly desirable for applications that are sensitive to grain boundary issues and require large-area or low-temperature growths which preclude using crystalline materials—displays and flexible electronics are common applications with such requirements. An important emerging application space (which will be the focus of the majority of this discussion) is back-end-of-line (BEOL)-compatible electronics. By the end of a conventional complementary metal-oxide-semiconductor (CMOS) fabrication process, the device layer is sensitive to thermal degradation at a much lower temperature than the initial wafer. A thermal budget for any further processing of in general no more than 400 °C is imposed. It is highly desirable to integrate additional functionality (i.e., logic, memory, or sensing) in the back end of line—anything that can save chip space is enormously valuable in an era when Moore's law is running up against fundamental physical limits—however, it is very challenging to integrate a high-performance material in a manufacturable and scalable way with such a tight thermal constraint.

Without resolving the degeneracy and crystallinity issues, binary indium oxide cannot be useful for BEOL devices despite

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its many other promising qualities. It has been well-known since 2004 that amorphous oxide semiconductor (AOS) materials can offer moderate electron mobilities on the order of 10 $cm^2\ V^{-1}\ s^{-1}$[9] (and up to several times higher with subsequent optimization), however amorphous indium oxide offers electron mobility up to ≈100 $cm^2\ V^{-1}\ s^{-1}$ which should result in much better device performance. It has recently been found that greatly reducing the thickness of indium oxide (and the larger class of AOSs) down to the low-single-digit nanometer scale can resolve the issues and allow new AOS channel materials with superior mobility to emerge. This review will focus on the device-level progress toward truly high-performance low-thermal-budget AOS transistors with near-ideal subthreshold swing (SS), record on-current among even conventional semiconductors, negligible off-current, enhancement-mode operation, and more with promise for integration into CMOS processes as high-performance logic or memory with back-end-of-line compatibility.

The remainder of this introduction will briefly review the history leading to the re-emergence of indium oxide as a semiconductor channel material. Section 2 serves as a review of fundamental properties that enable high-performance amorphous oxide electronics. Section 3 gives a brief overview of available growth techniques with a focus on atomic layer deposition (ALD) which is especially suitable for the fabrication of high-performance BEOL-compatible indium oxide devices. Section 4 reviews the state-of-the-art in device research, while Section 5 is dedicated to the bias stability behavior of the devices. Section 6 contains closing remarks.

1.1. History

The first answer to the issues of indium oxide outlined above (degeneracy and crystallinity) was driven by the display industry applications and was to incorporate additional metal cations in significant proportion into the binary metal oxide (most commonly zinc and gallium are used, but many others have been investigated[10,11]). The inclusion of these additional cations both helps to suppress the carrier concentration and promotes amorphous growth. The physical mechanism behind the carrier suppression is thought to be stronger binding of oxygen (whose vacancy is widely thought to act as a double donor) due to the high ionic potential of the dopant metal atoms,[12] and it has been observed that the incorporation of multiple cations with different radii and ionic potentials is effective at suppressing crystallinity.[13] While this solution is very effective at addressing the issues, the trade-off is that the carrier mobility is reduced (by up to an order of magnitude) from that of the parent binary indium oxide. Regardless, the discovery of this was a major breakthrough and spawned the modern field of AOS research. With material characterization first reported in 2001,[14] the watershed moment came in 2004 with the report of an amorphous indium-gallium-zinc-oxide (IGZO) channel transistor with an electron mobility around 10 $cm^2\ V^{-1}\ s^{-1}$.[9] A flurry of subsequent development followed with rapid commercialization in displays by 2012.[15] High-mobility amorphous semiconductor materials have been a long-standing problem for many applications. Prior to IGZO, the best performing and most mature amorphous semiconductor by far was amorphous hydrogenated silicon (a-Si:H) which can achieve electron mobilities up to ≈1 $cm^2\ V^{-1}\ s^{-1}$ at best. Organic semiconductors, widely seen at the time as a potential replacement for a-Si:H, offered similar performance (e.g., see ref. [16]) after a great deal of research effort. High carrier mobility is critical for electronic device applications as it is intimately related to the achievable on-state current, transconductance, and speed of operation. For the aforementioned display industry applications, a higher-mobility amorphous channel material was needed to support greater pixel densities and refresh rates.[17]

For CMOS BEOL and monolithic 3D (M3D) integration applications which are the main focus of the remainder of this review, high mobility is likewise crucial. The goal of a BEOL device process is to integrate additional logic or other functionality (e.g., memory, sensing, or power management) directly atop a fabricated chip. Since this integration requires a greatly reduced thermal budget to not damage the devices in the Si CMOS layer (generally <400 °C), it proves very difficult to obtain a suitable high-performance material, especially in a large-scale manufacturable way. The class of transition and post-transition metal oxide semiconductors, and especially indium oxide which has the highest mobility among them, become ideal candidates for these applications once their potential issues are addressed and resolved.

2. Properties of Indium Oxide

2.1. Structural

In its crystalline form, indium oxide almost exclusively adopts a body-centered cubic bixbyite structure ($a \approx 1.0117$ nm, space group $Ia\bar{3}$[18]) illustrated in **Figure 1**a. Its rather large 80-atom unit cell is an ordered arrangement of smaller polyhedral units of indium atoms coordinated with six oxygen atoms, highlighted in Figure 1b. When amorphous, the polyhedra are retained but with more corner sharing and less edge sharing.[19,20] The present understanding of amorphous indium oxide physical structure is reviewed in Ref.[21] Aside from the bixbyite form, there are sparse reports of a rhombohedral indium oxide structure with space group $R\bar{3}C$,[22–24] but it has only been observed following the application of high pressures or by careful epitaxial growth, and is metastable. A third polytype with space group $I2_13$ has been predicted but not observed experimentally.[25,26]

Thinning indium oxide into the single- and sub-nanometer regime appears to encourage amorphous growth.[27,28] It is not trivial to assess the crystallinity of such a thin layer, and the best evidence at present is high-resolution transmission electron microscopy (HR-TEM) images of the cross sections of such ultrathin layers, shown in Figure 1c, or grazing-incidence wide-angle x-ray scattering (GIWAXS)[28] which have shown no signs of crystallinity. This is consistent with observations on other materials and in particular oxides, such as Al_2O_3,[29] HfO_2,[30] TiO_2,[31] TiN[32,33] In the HfO_2 study referenced, the annealing temperature required to crystallize the layer increases rapidly with decreasing thickness. Likewise, in the TiO_2 study referenced no crystallinity could be detected in thinner layers at any annealing temperature.

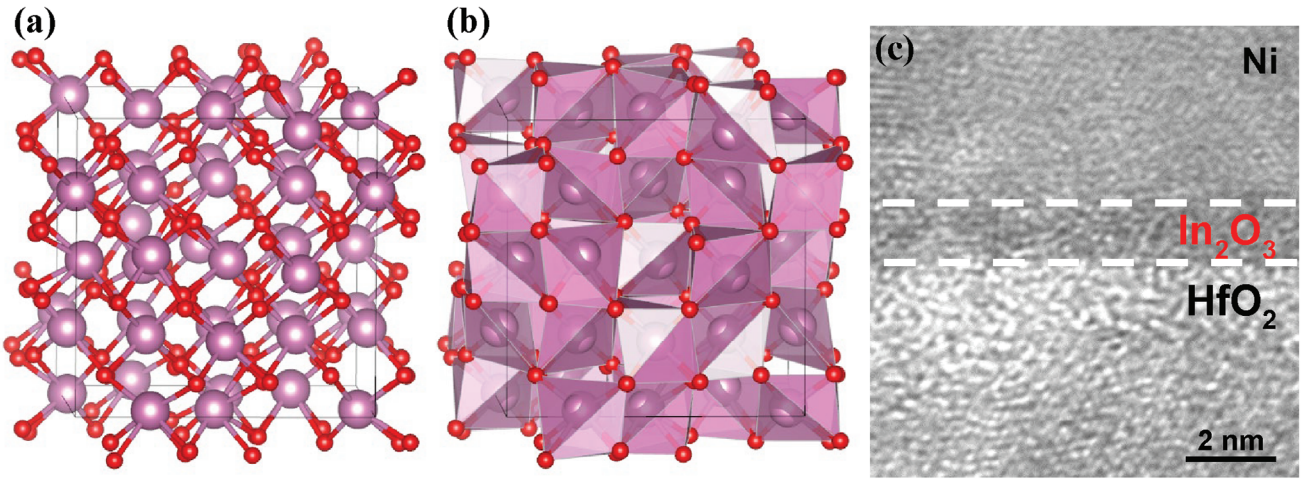

Figure 1. The atomic structure of crystalline indium oxide. The red atoms represent oxygen and the purple atoms represent indium. a) Ball-and-stick model. b) Model highlighting InO_6 polyhedra. The unit cell is indicated by the thin black lines. c) HRTEM image of a 1.2 nm thick ALD-grown indium oxide layer showing no evidence of crystallization. Adapted from ref. [111]. Crystal structure renderings were produced using VESTA[138] with data from the Crystallography Open Database.[139]

2.2. Electronic

The electronic band structure of indium oxide has features that are not seen in commonly studied semiconductors that are key to understanding its suitability for the applications discussed. These killer features are its 1) resistance to disorder and 2) degenerate charge neutrality level (CNL). Much of the following literature discussion refers to research on crystalline indium oxide samples. The electronic structure of amorphous indium oxide is relatively unstudied with only a handful of experimental results to draw from. However, the electronic structure of crystalline In_2O_3 can be used as a good approximation of amorphous In_2O_3 because it is well-known the electronic structure of AOSs is insensitive to local structural randomness because their conduction bands are made of spherically extended s orbitals of metal cations.[13] Therefore, as a result, many of the electronic properties of In_2O_3 appear to be preserved in amorphous form.

The bandgap of bulk bixbyite indium oxide is ≈2.7 eV and is direct.[34–37] There are many conflicting reports in the literature that suggest a bandgap about 1 eV larger than this based on optical measurements (i.e., Tauc's method), which has resulted in confusion about the true value due to the large discrepancy. The reason for the large inconsistency is twofold: 1) the direct optical transition from the valence band maximum to the conduction band minimum is parity forbidden[34] and 2) due to the uncontrolled degenerate carrier concentration there may be unaccounted for Burstein-Moss shift in many experiments, that is, the lower portions of the conduction band may be completely filled. In fact, this significant degree of conduction band filling is exploited in angle-resolved photoemission spectroscopy measurements to determine the true bandgap experimentally in bulk crystalline samples.[36,37] To date only one theoretical study has explored the changes to electronic structure brought about by extreme thinning. Si et al. find that in the nanometer thickness regime, quantum confinement widens the bandgap, which helps to suppress the degenerate carrier concentration.[27]

A variety of experimental[27,38] and theoretical[39–41] results demonstrate that the electronic properties of indium oxide are robust against disorder. For example, detailed molecular dynamics and density functional theory (DFT) calculations predict negligible changes to the character of the conduction band with increasing amorphization,[39] for example, a <5% change in electron effective mass. It should be noted that the theoretical works often predict a dramatic bandgap reduction with increasing amorphization. Experimental measurements on amorphous indium oxide still show evidence of a wide bandgap of consistent magnitude with the crystalline form.[42,43] As a result of this robustness, unlike typical materials there is minimal correlation between its transistor mobility and the process thermal budget, as shown in **Figure 2**. The method of growth and details of a

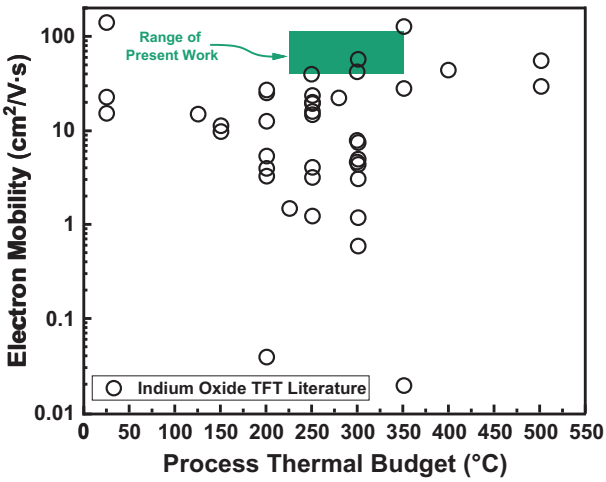

Figure 2. Survey of the reported transistor mobilities of indium oxide TFTs in literature as a function of the process thermal budget. The green bar indicates the range explored in the reviewed work. Literature values are from Refs. [57,58,60, 150, 161, 169–194]; see also Table S1, Supporting Information.

specific fabrication process remain determining factors. This robustness is a very unintuitive result; in silicon, for example, the electron mobility is reduced by around three orders of magnitude in amorphous form. Experimentally, the electron mobility in indium oxide (and in related metal oxides) is only moderately reduced in amorphous form (e.g., in the worst case by about 50% when compared to the highest quality single-crystal indium oxide with low doping[44]). Several angles have been proposed to understand this phenomenon. Early work by Bellingham et al. studied transport in amorphous indium oxide and ITO films, finding ionized impurity scattering to dominate the mobility rather than any structural disorder mechanism.[38] In fact, it was found that the mean free path due to structural scattering was roughly 10 nm, two orders of magnitude larger than the interatomic spacing. This result was interpreted by noting that the wavelength of the electrons at the Fermi surface was around 3 nm and as a result, the rapidly-varying atomic potentials due to the disorder may be effectively smoothed out or screened.[38] Perhaps the most intuitive argument, given by Nomura et al.[45,9] relates to the physical character of the conduction band in real space. In general, the widely studied semiconductors (i.e., Si, Ge, III-V's) have conduction (and valence) bands whose characters are primarily derived from p-orbitals with their highly directional dumbbell shape. When these p-orbitals are well-aligned as in a perfect crystal lattice, there are continuous straight paths for electrons to conduct along. When that order is perturbed, the efficient straight paths are no longer present resulting in greatly increased rates of scattering, to say nothing of carrier localization effects. In the transition metal oxides, the conduction band is primarily of spherically symmetric ns-orbital character with larger n (4 or 5) and hence large radius. The symmetry conveys a high degree of immunity to angular disorder, and the relatively large radii help to ensure consistent orbital overlaps between neighboring metal cations allowing for consistent efficient conduction paths even when the structural order is greatly perturbed. A more formalized argument along these lines is given by Robertson.[46,47] The effective Bohr radii a^* of the AOSs are large. The effective Bohr radius is given by,

$$a^* = \frac{a_0 \epsilon_r}{m_e^*/m_e} \tag{1}$$

where a_0 is the Bohr radius of hydrogen, ε_r is the relative permittivity, m_e^* is the electron effective mass, and m_e the electron mass. Taking the most reliable known values for bixbyite indium oxide ($\epsilon_r \approx 10.55$[48] and $m_e^* = 0.18\, m_e$ near the bottom of the conduction band[37,49]) gives an estimated a^* of 3.1 nm. It is likely that the permittivity of amorphous indium oxide differs somewhat, but it is unimportant for this example calculation. The result of this large value is that the mobility edge—the energy level in a disordered material above which states are conductive (de-localized) and below which states are localized and do not contribute to current flow—occurs at a relatively low density of states. This can be understood by the Mott criterion,

$$a^* \cdot \sqrt[3]{n_c} = 0.26 \tag{2}$$

where n_c is a critical carrier concentration above which the material becomes conductive and below which the material behaves as an insulator. With the large effective Bohr radius of 3.1 nm, a critical concentration of 5.9×10^{17} cm^{-3} is found with Equation (2). Above this very moderate carrier concentration, the energy is sufficient to de-localize. As a result, it is easier to turn AOS transistors on (i.e., no limitation is placed on the subthreshold swing by disorder) compared to traditional amorphous semiconductors like a-Si:H whose critical concentration is $\approx 10^3$ times higher since far fewer immobile states must be filled before the onset of conductivity. By the same token, decreasing the carrier concentration below the critical value n_c by modulating the In_2O_3 with a voltage will rapidly move the Fermi level below the mobility edge and into the localized states, resulting in the cessation of conductivity.

The CNL is thought to play an unusually important role in the electronic properties of indium oxide due to its uncommon location within the conduction band at $\approx E_C + 0.4$ eV in bulk.[50] Also widely referred to as the branch point energy, the CNL is the demarcation point above which the dominant surface states are electrically neutral if empty and are called acceptor-like, and below which the dominant surface states are electrically neutral if filled and are referred to as donor-like. Since it is energetically preferred to maintain charge neutrality, the Fermi level therefore tends to align with the CNL at the surfaces and interfaces of a material, resulting in widely observed band-bending. This can occur by a defect generation process, and is thought to be a culprit of the Fermi level pinning issue that plagues many promising semiconductor materials—at the interface with the metal contacts, the Fermi level can become pinned near the middle of the bandgap due to unfortunate alignment of the CNL, resulting in a large Schottky barrier (Φ_B) which ruins the Ohmic contact performance, irrespective of metal workfunction (ϕ_M) alignment. In practice, whether this is an issue or not for a given material depends on both its CNL alignment and its dopability. Further details can be found in the works of Tersoff.[51] and Robertson[52] In general, the CNL location is determined by the balance of the valence to conduction band density of states. The large valence band density of states of indium oxide (**Figure 3**b) causes its CNL to be located deep inside the conduction band.[50,53] This results in degenerate surfaces and interfaces with very low contact resistance, and when interpreted through the amphoteric defect model can explain indium oxide's propensity for degenerate n-type doping in the bulk.[50,54] The high location of the CNL can also explain why the Fermi level can be raised into and held in the conduction band without resulting in compensating defect formation, an important issue for a-Si:H.

Controlled doping in indium oxide is generally accomplished by managing native defects rather than by the intentional incorporation of a substitutional element as in conventional semiconductors. By manipulating the conditions during growth, the doping levels can be controlled over a wide range (but with a high floor around 10^{17} cm^{-3}). Defects are discussed in more detail in the following subsection. While indium oxide has a strong propensity for degenerate n-type doping, p-type doping is not feasible for a variety of reasons. This is a general problem among oxide semiconductors with few exceptions—the valence bands tend to be flat (low mobility), derived from O 2p orbitals (and thus not resistant to disorder), lie very deep below the vacuum level (making it difficult to have shallow p-type dopants), and the materials

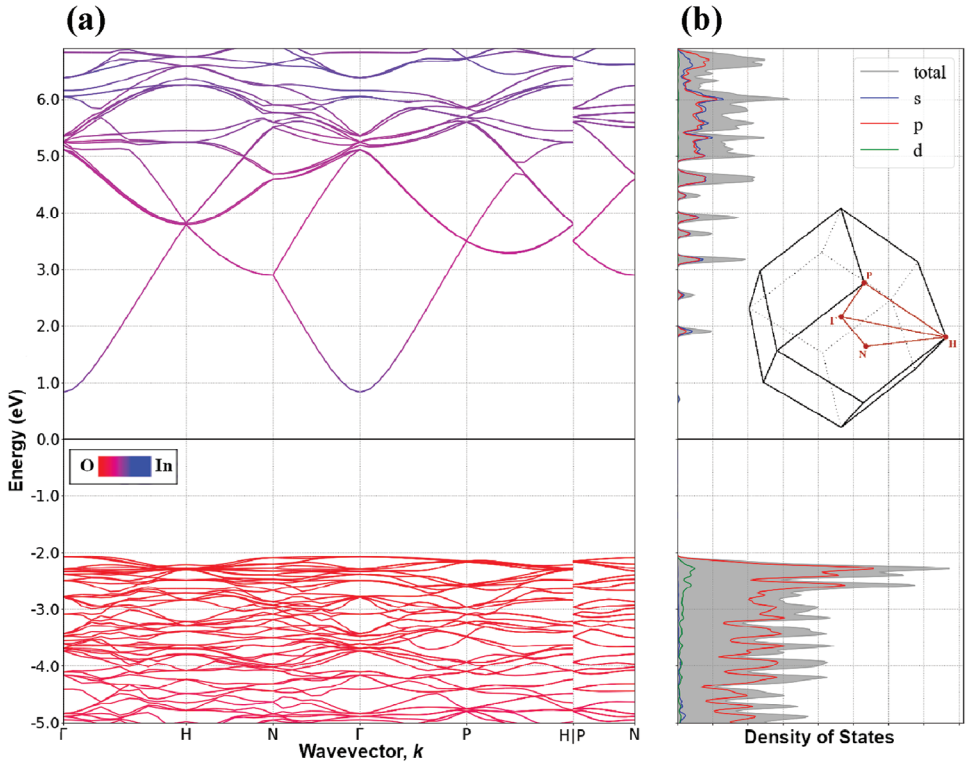

Figure 3. Theoretical a) atom projected band structure and b) orbital projected density of states of bulk bixbyite indium oxide calculated by DFT. Inset shows the first Brillouin zone with high-symmetry points labeled. A single conduction band valley with low effective mass is predicted at the Γ-point, which is largely of In 5s character. Data from the Materials Project[140] and further processing with the Materials API.[141] The bandgap has been manually corrected by a scissor operation.

have limitations on their dopability (i.e., compensation) that preclude moving the Fermi level close to the valence band.

In summary, despite being amorphous, indium oxide can largely retain its high electron mobility due to s-orbital symmetry. A further advantage is that it is easy to rapidly modulate the conductivity of amorphous indium oxide because it has dramatically fewer disorder-induced gap states than traditional amorphous materials, and it is easy to strongly modulate the conductivity (i.e., to move the Fermi level deep into the conduction band or deeply above the mobility edge) because the defect compensation mechanism of a-Si:H is not present. It is a wide-bandgap semiconductor with a direct gap that grows larger in very thin layers due to quantum confinement. Its uncommon CNL location makes Ohmic contacting extremely easy and can contribute to the carrier degeneracy. Since having a very thin layer of indium oxide reduces its carrier degeneracy and encourages amorphization for which there are minimal penalties, it presents the possibility for high-performance amorphous oxide devices.

2.3. Defects

Indium oxide is a defect-rich material like most oxide semiconductors. As will be discussed in Section 3, it generally has a background carrier concentration of at least $n = 10^{17}$ cm^{-3} even with the most careful high-quality growth methods available. The dominant defect has been a source of debate, with oxygen vacancies (v_O), hydrogen interstitials (H_i), and substitutional hydrogen in the place of oxygen (H_O) being the most common contenders. Occasionally indium interstitials (In_i) are also suggested as the dominant donor.[55] As in the previous subsection, the current experimental evidence suggests that the discussion applies equally well to both amorphous and crystalline forms, although the terms such as interstitial lose their strict meaning without a crystal lattice.

Going back to the earliest growths of indium oxide, a strong correlation has been noted between oxygen partial pressure during growth and the carrier concentration of the resulting material, with oxygen-deficient growth environments yielding the highest carrier concentration.[56–60] Stoichiometric analyses likewise find a correlation between increased oxygen vacancies and increased conductivity.[57,58,60] As a result of this clear correlation, oxygen vacancies (v_O) have long been considered the dominant defect in indium oxide (with similar results on the other oxide semiconductors). From a thermodynamic perspective, a fundamental reason for this is the relatively low dissociation energy of the In—O bond of 346 ± 30 kJ mol^{-1} (3.59 ± 0.32 eV per molecule) in bulk.[61] The rather stable Si—O bond, for comparison, has a dissociation energy of 799.6 ± 13.4 kJ mol^{-1} (8.29 ± 0.14 eV per molecule).[61] There is widespread agreement that v_O defects act as double donors, however from the theory side there are disagreements about the energetics of v_O formation depending on the selection of functional and estimation of the bandgap. Some studies find that v_O are shallow donors for Fermi

levels up to roughly the conduction band edge,[62,63] while others find that they are deep donors.[55,64] A small review is given in the most recent work in ref. [63]. Recent theoretical work suggests that the energy required to form an oxygen vacancy decreases significantly near the surface.[65] An emerging school of thought stemming from this result is that the n-type doping of all indium oxides (and other n-type oxides) may originate from surface-adjacent oxygen vacancies,[66,67] which squares well with the prior CNL discussion.

Secondary to oxygen vacancies, hydrogen interstitials (H_i) or substitutional hydrogen in the place of oxygen (H_O) are also somewhat frequent candidates for the dominant donors. Theoretical calculations predict both H_i and H_O to be single donors, and the formation of these defects is sometimes predicted to be energetically favorable over v_O for Fermi levels high in the bandgap.[68,69] Experimentally, hydrogen-rich bulk indium oxide has been found to have carrier concentrations proportional to hydrogen levels,[70–72] and fairly compelling muon spin resonance spectroscopy (μSR) measurements (using muons as proxies for hydrogen) have shown a strong preference for single electron donation with a fairly shallow ionization energy between 47 and 94 meV.[69]

A third option occasionally found in literature attributes the n-type doping to indium interstitials (In_i). Ref. [55] for example, predicts that oxygen vacancies lie too deep in the bandgap to act as efficient donors, but instead assist in the indium interstitial electron donation process.

2.4. Optical

Owing to its wide bandgap, indium oxide is largely transparent to optical wavelengths of light like many other oxide semiconductors. In typical thin films and in bulk, the optical transmittance is generally around 70–80% with an index of refraction around 2.0 (e.g., ref. [73]). Very thin layers can have near-unity optical transmittance while retaining their high conductivity, making them useful for transparent interconnects in optoelectronic devices.[60] Indium tin oxide (ITO) is also widely used commercially for similar purposes.

2.5. Mechanical and Thermal

Indium oxide has suitable mechanical and thermal properties that do not constrain its application in electronic devices. It is very thermally stable, with a melting point around 1912 °C in crystalline bulk form.[74] Its thermal conductivity is moderate—up to 20 $W{\cdot}m^{-1}{\cdot}K^{-1}$ in high-quality single crystals,[75] and lower but still manageable in less-ordered forms. Device thermal performance can be improved by integrating high thermal conductivity materials.[76] Its thermal expansion has been fit as $\Delta a/a_{RT} = (7.20 \pm 0.06) \times 10^{-6}{\cdot}T + (1.15 \pm 0.08) \times 10^{-9}{\cdot}T^2$ based on powder X-ray diffraction measurements where a is the lattice constant and a_{RT} is the room temperature value.[77]

3. Growth of Indium Oxide

For the reasons and applications described, a growth method with extreme repeatable thickness control is required. It should produce high-quality material, and be scalable and economically viable. The various methods used to grow indium oxide are briefly reviewed here before switching focus to ALD, which is especially well-suited for the current needs.

For obtaining bulk material, a high-quality melt-based growth technique termed the levitation-assisted self-seeding crystal growth method (LASSCGM) was reported in 2014,[78] and is the first major advancement in bulk indium oxide growth since the 1960′s. Thus far, it has been able to yield single-crystal indium oxide wafers up to 3 cm in diameter which are of sufficiently high quality to be used as molecular beam epitaxy (MBE) substrates for the growth of other materials.[79] Aside from LASSCGM, the existing bulk growth methods are hydrothermal,[80] vapor oxidation,[81] flux,[82] and chemical vapor transport (CVT).[83] Among these, the flux and CVT methods are both relatively easy to implement and produce moderately sized (≈3 mm–1 cm scale) single crystals of high quality and thus are still frequently employed.

Indium oxide thin-film growth methods are much more diverse. Although epitaxial growth has been attempted by a variety of methods (including MBE[84] and plasma-assisted MBE,[35,44,85] pulsed-laser deposition (PLD),[86,87] pulsed electron-beam deposition (PED),[88] and metalorganic chemical vapor deposition (MOCVD)[89–92]) and on a variety of substrates, high-quality single crystal layers have proved difficult to obtain. At the other extreme, it is also difficult to obtain amorphous films. As discussed in Section 1, binary indium oxide has a strong tendency to form small crystal domains which can range from ≈10 nm diameter to micrometer scale depending on the growth technique. Nominally amorphous thin films have been obtained by ion beam sputtering (IBS),[38,42] PLD,[20] and MOCVD[93] among others.

The desire for high-quality indium oxide without grain boundaries, with a low (<400 °C) thermal budget, and the discovery that very thin layers promote amorphization and help to control the carrier concentration leave very few candidates for suitable techniques. In this regime of interest, ALD meets the criteria excellently. ALD is a subset of chemical vapor deposition (CVD) in which the growth is self-limiting. With moderate substrate heating (typically <300 °C) under vacuum, precursors are flowed into the ALD chamber, one at a time, where they react with the substrate surface to form a highly uniform atomically-thin coating, generally via a ligand exchange process. This process continues sequentially, precursor by precursor, until the target thickness of material is achieved. ALD offers excellent uniformity and conformality on 3D structures over arbitrarily large substrate areas with a relatively low thermal budget. A very wide range of materials can be grown by ALD, including metals, semiconductors, and dielectrics, with a wide range of precursor chemistries available for common materials. The reported growth rates and ALD windows for the indium oxide ALD chemistries in literature are summarized in **Figure 4**. Of these, several have been applied successfully in the fabrication of electronic devices. The trimethylindium (TMIn) + H_2O chemistry is used in many of the referenced works since TMIn is readily available as a commercial MOCVD precursor. A diethylmethylindium (Et_2MeIn) chemistry has recently been studied for similar ultra-thin high-performance devices,[94] and more recently a very low-temperature (down to 35 °C) ALD chemistry has been developed using a dimethyl[N-(tert-butyl)−2-methoxy-

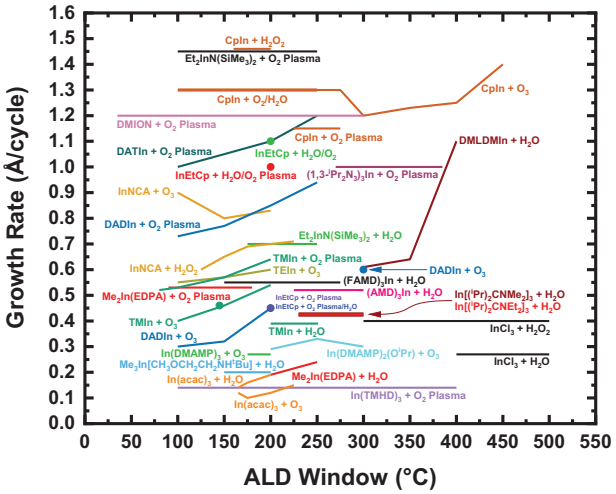

Figure 4. Reported successful ALD growth processes for indium oxide from the literature. Colors are added for visual clarity and do not have further significance. Literature values are from Refs. [56,58,60,94,95, 146–168, 222–225]; see also Table S2, Supporting Information.

2-methylpropan-1-amine]indium (DMION) precursor[95] which may enable an even wider range of substrate compatibility.

4. High-Performance Ultra-Thin Metal Oxide Transistors

As alluded to in the previous sections, recent work on the metal oxides has highlighted a very interesting trend: extremely thin channel layers of the amorphous metal oxide semiconductors, in general, are able to achieve excellent device performance. The almost-atomically-thin channel body offers exceptional electrostatic control at scaled channel lengths (equivalent to 2D materials) while, the resilient electronic structure of this class of materials preserves their high mobilities in amorphous form. In oxides that tend to crystallize, the extreme thinness can promote amorphization to reduce grain boundary issues, and in oxides that tend to degenerate like indium oxide and ITO the extreme thinness can reduce the carrier concentration to a manageable level that can be controlled effectively by electrostatic gating. In addition to pure indium oxide, work in this area has been reported in IGZO,[96,97] ITO,[100,98,99] indium tungsten oxide (IWO),[101,102] zinc oxide,[103] titanium oxide,[104] indium aluminum zinc oxide (IAZO),[105] with record-level performance frequently being reported after thickness scale-down. For indium oxide, functional devices have been fabricated with layers as thin as 0.5 nm,[106] but the best performance is generally found at between 1.2 and 3.5 nm thick in the established process. The thickness can be very precisely controlled in a scalable, repeatable manner due to the high-quality ALD growth (Section 3).

When the thickness of traditional semiconductor materials is scaled aggressively, for example, below 5 nm, typically their performance in electronic devices is severely degraded. For silicon in this thickness regime, the mobility (μ) rapidly decreases as the sixth power of thickness, that is, $\mu \propto t^6$[107] due to increased rates of scattering from surface effects. It can be speculated that there may be two reasons why indium oxide and related oxides are immune to this. For one, the t^6 dependence is derived mainly from surface roughness[108] and the ALD indium oxide studied is atomically smooth. More fundamentally, it has been established that the conduction band in these materials is very robust against disorder. The conduction band electrons lie in In 5s-derived extended states and as a result, may be less sensitive to surface variations. Due to its special CNL alignment, electrons are accumulated at the oxide surface, in contrast to conventional semiconductors.

4.1. Fabrication

Fabrication process flows have been described in detail in the cited device literature. For the ultra-thin indium oxide devices, a typical process is outlined in **Figure 5**a. A photograph of a completed 4-inch wafer of devices and a cutaway illustration of a typical device structure are shown in Figure 5b,c. A few points warrant particular attention. The thermal budget of this typical process is just 225 °C, well below the limits for BEOL processing and even low enough for processing on certain plastic substrates. Using alternative ALD chemistries, there is potential to further reduce this as needed (Figure 4). Both the gate dielectric and channel materials are grown by mature ALD processes, resulting in simple fabrication and low densities of interface traps. ALD Al_2O_3 and HfO_2 have been studied for the dielectric, with HfO_2 preferred due to its higher dielectric constant. Sub-nanometer equivalent oxide thickness (EOT) has been reported in devices with ALD HfO_2 dielectrics,[106] allowing for excellent electrostatic control of the channel. Due to the preferential CNL alignment, the source and drain Ohmic contact fabrication is very simple; no complicated optimization of metal stacks, annealing routines, or implantations are required unlike for many other semiconductors. Typically, evaporated nickel is used and yields very low contact resistance (R_C, as low as 0.03 Ω•mm) and specific contact resistivity (ρ_C, as low as 3×10^{-9} Ω•cm^2) on its own, however to date no detailed contact optimization study has been reported. Finally, the indium oxide is also easily wet etched by concentrated HCl with excellent selectivity against HfO_2, or can by dry etched by BCl_3/Ar plasma in ICP-RIE. The developed fabrication processes are robust and generally have ≈100% device yield at wafer scale with small device-to-device variation, and depending on the process can be completed with as few as three lithography steps for rapid prototyping.

4.2. DC Electrical Performance (As Fabricated)

Representative transfer and output curves are shown in Figure 5d,e. The device shown has remarkable DC performance, achieving an on-current (I_{on}) greater than 2 A mm^{-1} with a large I_{on}/I_{off} ratio on the order of 10^6, limited only by gate leakage. Statistical characterization is shown in Figure 5f–j, which shows the thickness dependence of key DC parameters as the channel length is aggressively scaled. One issue worth mentioning is the threshold voltage (V_T): in order to have enhancement-mode operation ($V_T > 0$ V) which is highly desirable for logic devices, the channel thickness must be reduced which significantly reduces I_{on} at a given channel length. Further details are available in ref.

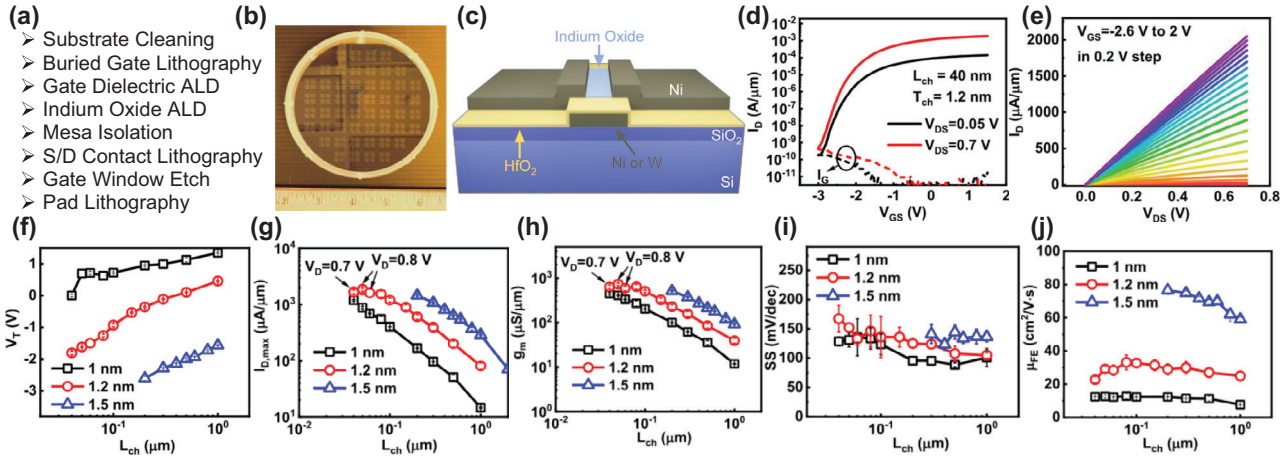

Figure 5. Fabrication and DC electrical characterization of typical indium oxide devices. a) Outline of a typical fabrication process. b) A 4-inch wafer of fabricated devices. c) Illustration of a typical indium oxide TFT device structure. d) Transfer and e) output curves of a representative scaled indium oxide device with no post-treatment. A large on-current above 2 A mm^{-1} is achieved. Statistical characterization across a variety of channel lengths and thicknesses of f) threshold voltage, g) maximum drain current, h) transconductance, i) subthreshold swing, and j) field-effect mobility. A wide range of high-performance devices are possible even without post-treatment.

[109]. A solution to this is to apply a post-fabrication treatment, discussed in the following section.

4.3. Post-Fabrication Treatment

Several post-fabrication treatments have been investigated to address the enhancement-mode performance trade-off. Broadly speaking, oxygen annealing[110] and oxygen plasma exposures[111] are effective at shifting V_T positively and have the added benefit of reducing SS. It is understood that oxygen treatments are effective to reduce the oxygen vacancies and oxygen-related defects in In_2O_3 to achieve a positive V_T shift and a significant reduction on SS. Encapsulation schemes generally make V_T more negative, or at best result in minimal shift. This is a potential problem for top-gate In_2O_3 transistors especially during high-k deposition by ALD at high temperatures. This is because metal precursors for high-k take oxygen away from In_2O_3 film, leaving oxygen vacancies and causing the increase of carrier density. Such problems can partly be alleviated by oxygen treatments after device fabrication.[76] An example of the case of oxygen plasma treatment is shown in **Figure 6**.

4.4. Ultra-High Current

Indium oxide has a remarkable upper limit to its current carrying capacity. Recently, deeply scaled ALD In_2O_3 transistors have been reported with record-high drain currents exceeding 10 A mm^{-1},[112,113] an order of magnitude above typical high-performance semiconductor channel benchmarks and 2–3 times higher than previous records. A record high transconductance among all planar transistors of 4 S mm^{-1} is also achieved, as shown in **Figure 7**e. These results are obtained at moderate gate and drain biases in BEOL-compatible devices, although pulsed *I*–*V* measurements are used to mitigate self-heating effects. A HAADF-STEM image of the smallest studied device with 7 nm channel length is shown in Figure 7a. Sample measured transfer characteristics in semi-log and linear scales are shown in Figure 7b,c, respectively, with corresponding output characteristics in Figure 7d. These extraordinary results are enabled in part by extreme channel length scaling down to 7 nm, equivalent oxide thickness (EOT) scaling down to 0.77 nm, and very low contact resistance as a result of indium oxide's metal-like CNL alignment. Scaling the channel width can offer even further improvements.[113–115] However, device engineering alone does

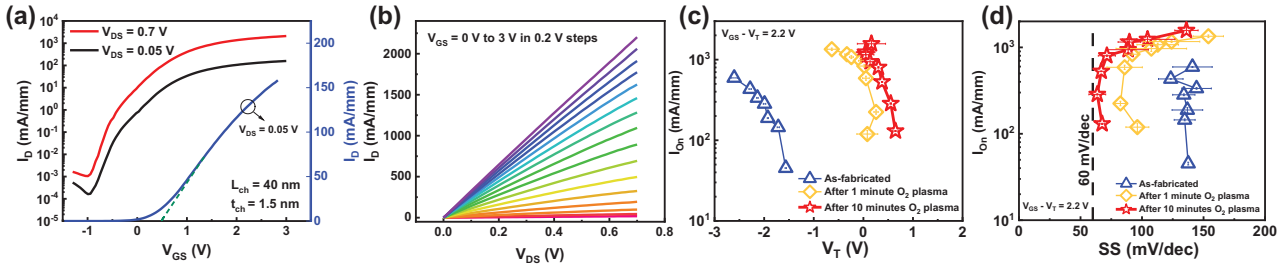

Figure 6. Effects of oxygen plasma post-fabrication treatment. a) Transfer and b) output curves of a scaled device demonstrating enhancement-mode operation with very high drain current over 2 A mm^{-1}. c) On-current plotted against threshold voltage demonstrating good scaling behavior with enhancement-mode operation at high on-currents. d) Subthreshold swing plotted against on-current demonstrating excellent channel electrostatic control down to short channel lengths with high on-current. Error bars represent one standard deviation from the average of at least 5 devices.

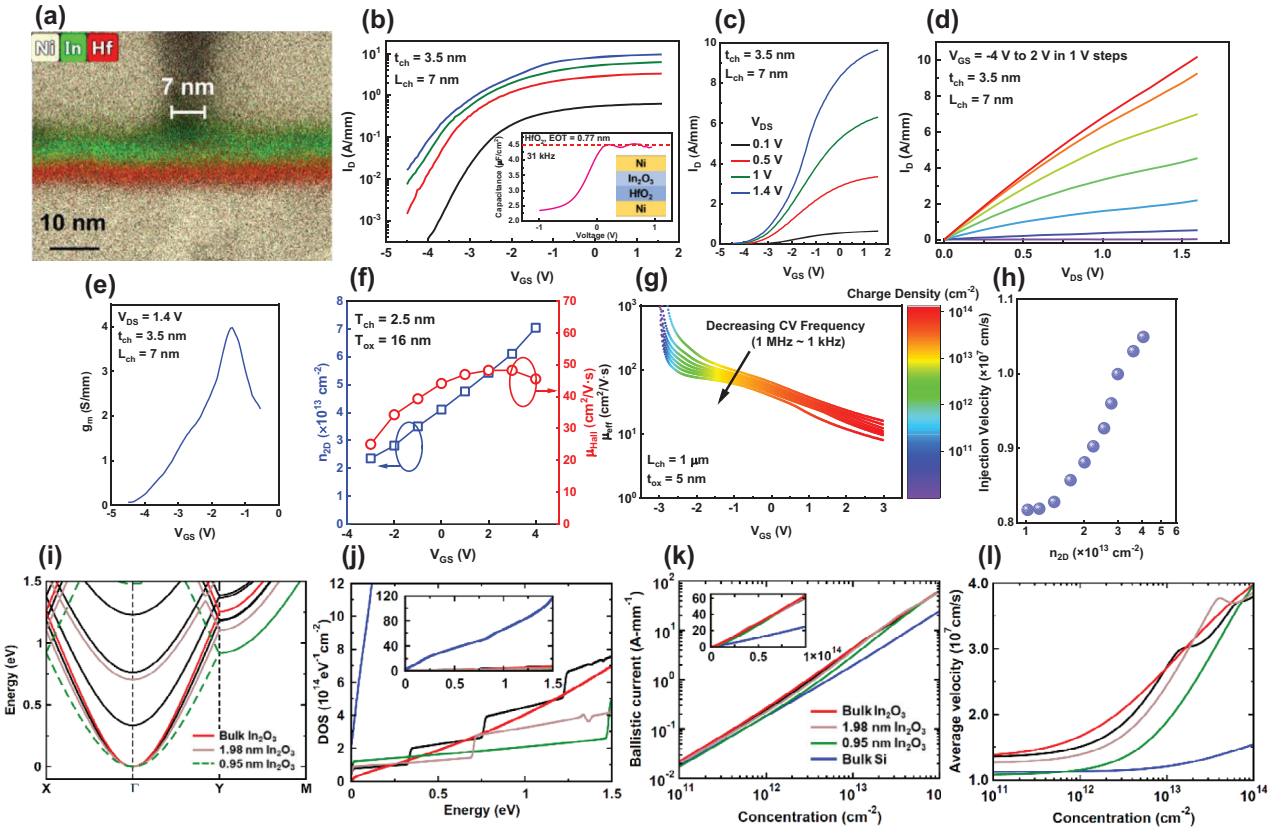

Figure 7. Performance of extremely scaled indium oxide transistors. a) HAADF-STEM cross section with EDX mapping of a device with 7 nm channel length. Transfer curves of a 7 nm device in b) log and c) linear scales. d) Corresponding output curves. High-current measurements are collected with pulsed *I*–*V* measurements to mitigate self-heating effects. Inset of (b) shows *C*–*V* characterization of the gate stack revealing 0.77 nm EOT. e) Transconductance. f) Gated Hall effect measurement demonstrating high mobility at high carrier concentrations. g) Complementary split *C*–*V* measurement. h) Carrier injection velocity estimated from Hall effect concentration and transfer curves. i) Calculated band structures of bulk and ultra-thin indium oxide. j) Calculated density of states as a function of energy above the conduction band edge. Indium oxide has much lower available DOS, pushing carriers to occupy higher energy states. k) Calculated ballistic current versus electron concentration. At high concentrations, indium oxide can carry significantly more current than Si. l) Calculated average injection velocity as a function of the electron concentration for indium oxide and Si. As a result of its lower DOS, indium oxide is predicted to have significantly higher injection velocities at high carrier concentrations.

not explain the results: simultaneously high carrier density and velocity are key.

Hall effect measurements at room temperature find a high carrier density of 6–7 × 10^{13} cm^{-2} in the on state as shown in Figure 7f. Similar numbers are found by split *C*–*V* measurements, as shown in Figure 7g. Under the assumption of ballistic transport, that is, that the current is simply the product of carrier density and velocity, an estimation of the average injection velocity can be obtained as shown in Figure 7h. A velocity over 10^7 cm^{-1} s which increases at higher carrier concentrations is found. It is this simultaneous high carrier density and velocity, demonstrated for the first time in a nanometer-thick semiconductor transistor, which enables extremely high drain currents. The maximum drain current reaches 20 A mm^{-1}[113] with a gate-all-around nanoribbon structure.

The experimental results are well supported by DFT calculations of the density of states (DOS), carrier density, and average injection velocity as a function of the 2D carrier density (n_{2D}) as shown in Figure 7j–l, respectively. The simultaneous existence of high n_{2D} and high carrier velocity in In_2O_3 is attributed to its single nearly-isotropic conduction band with low effective mass located at the zone center, comprised of mostly In s-orbital character, as shown in Figure 7i. Its low DOS near the conduction band edge means that for a given carrier density the Fermi level (E_F) can be pushed deep inside the conduction band of In_2O_3 where electrons occupy high energy states. This leads to average velocity enhancement and high band velocity.

Benchmarking of key metrics for logic devices with the highest-performing (prioritized by on-current) 2D materials and traditional semiconductors to date is shown in **Figure 8**. Note that Figure 8a is supply voltage agnostic, and simply shows the maximum reported device current—while it would be preferable to give I_{on} at a standardized supply and gate overdrive voltage, the cited works often do not provide enough information to do so. For comparison purposes, the recently announced Intel 4 FinFET silicon CMOS process achieves an I_{on} of around 2.27 A mm^{-1} at a supply voltage of 0.7 V in nMOS devices.[116] The closest comparable published enhancement-mode indium oxide devices can achieve I_{on} around 0.6 A mm^{-1} under the same biasing

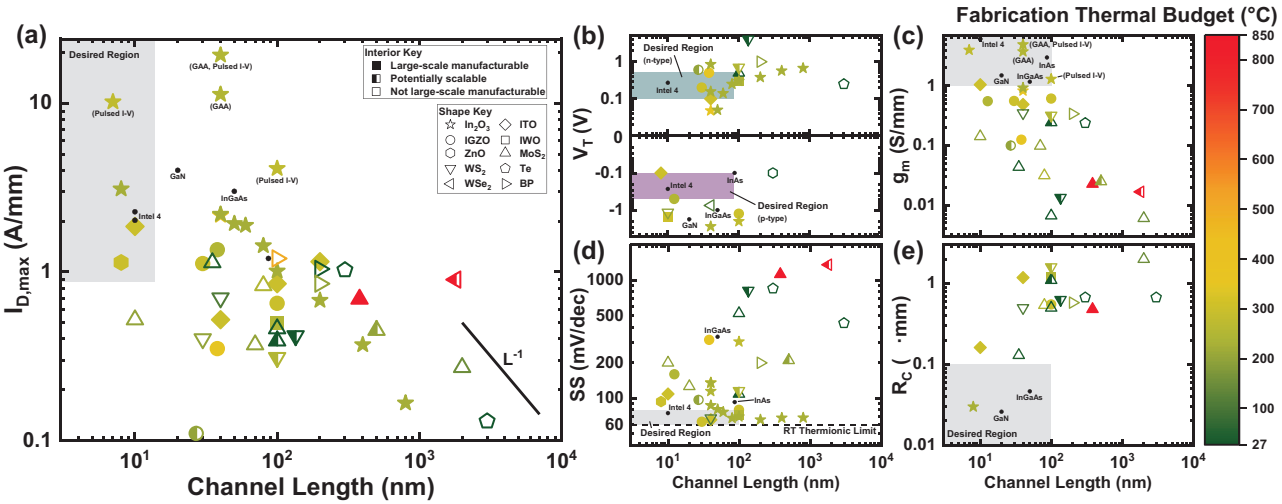

Figure 8. Benchmarking of high-performance semiconductor field-effect transistors for logic. a) Maximum achievable drain current. b) Threshold voltage. c) Transconductance. d) Subthreshold swing. e) Contact resistance. Colored shapes represent emerging high-performance low-thermal-budget materials where the color corresponds to the thermal budget and the shape corresponds to the material. Black dots represent traditional semiconductor materials. Not an exhaustive list. Values are estimated from available data when not explicitly provided. Shaded areas represent the most desirable regions of device operation for logic transistors. Data sources: indium oxide,[106,110–113] ITO,[100,142,99] IGZO,[143–146,97] IWO,[102,135] ZnO,[147] MoS_2,[148–156] WS_2,[157–160] Te,[161] WSe_2,[162] black phosphorus,[163–165] GaN,[166] InGaAs,[167] InAs,[168] Si.[116]

conditions[110] with disadvantages in process maturity, geometry (planar versus fin), and device scaling (40 nm channel length versus the 4 nm-equivalent node).

4.5. Others

Some initial studies into thermal management integration have been undertaken.[117,118,76] Despite the very low resistance of the devices, the tremendous on-current can be high enough to cause self-heating damage. It has been demonstrated that this can be largely mitigated by integrating phonon-matched thermally conductive materials into the device stack, allowing for even larger currents. The off-current has been estimated by careful temperature-dependent measurements as $\approx 6 \times 10^{-20}$ A μm^{-1} owing to indium oxide's wide bandgap, demonstrating promise for a BEOL memory selector or other ultra-low leakage application.[43] Despite the promising DC performance, if the devices cannot operate at reasonable speeds, they will not be useful. An initial RF performance study was conducted, realizing the highest reported f_T among all AOS transistors of 22.5 GHz and high f_{max} above 7 GHz.[119,120] RF performance can be further improved to f_T of 36 GHz by optimizing the device structure.[121] There is significant further room for improvement with deeper scaling below 150 nm channel lengths and by geometry refinements to minimize parasitics, however, even these relatively un-optimized devices demonstrated the ability to comfortably operate at CMOS-compatible speeds.

5. Bias Temperature Instability Behavior

Bias temperature instability (BTI) phenomena are shifts in the operating characteristics of a device that accumulate over time when subjected to applied voltage, elevated temperatures, or both. The larger the applied electric field and the higher the temperature, the more rapid the degradation. A variety of mechanisms can be responsible for BTI, but in general, charge trapping or de-trapping at interface and dielectric defects, or generation of new trap states (e.g., by the breaking of bonds) are the relevant phenomena. The physics of BTI is still not fully settled, even in the thoroughly studied case of Si.[122,123]

In a transistor, BTI is mainly observed as a change in the threshold voltage in response to gate biasing (although it may also simultaneously manifest in, for example, mobility degradation or increased subthreshold swing). Such changes are highly undesirable and great efforts have been undertaken to minimize BTI shifts in commercial devices to ensure stable operation over long timescales. Since it is a trap-related phenomenon concentrated around the channel and dielectric interface, engineering efforts have mainly gone toward optimized materials growth, gate stacks, and post-fabrication treatments such as annealing. Among oxide semiconductors another avenue for reducing the BTI shifts has been either adjusting the ratios of cations[124,125] or incorporating new cations into the material. This comes with the usual tradeoffs in mobility.[126] Since oxide semiconductor transistors are usually fabricated in a TFT geometry, the top surface of the channel material tends to be exposed to the environment. Encapsulating the channel with an appropriate passivation layer has been found to be an effective strategy.[127]

For positive gate bias stresses, generally the threshold voltage (V_T) shifts positively and vice versa for negative gate bias stresses. This is straightforward to understand since V_T is inversely related to the amount of charge present in the dielectric and at the interface traps; when a positive bias is applied to the gate the semiconductor bands bend downward resulting in electron trapping (negative charge accumulation), and when a negative bias is applied de-trapping occurs. The dielectric and interface traps have

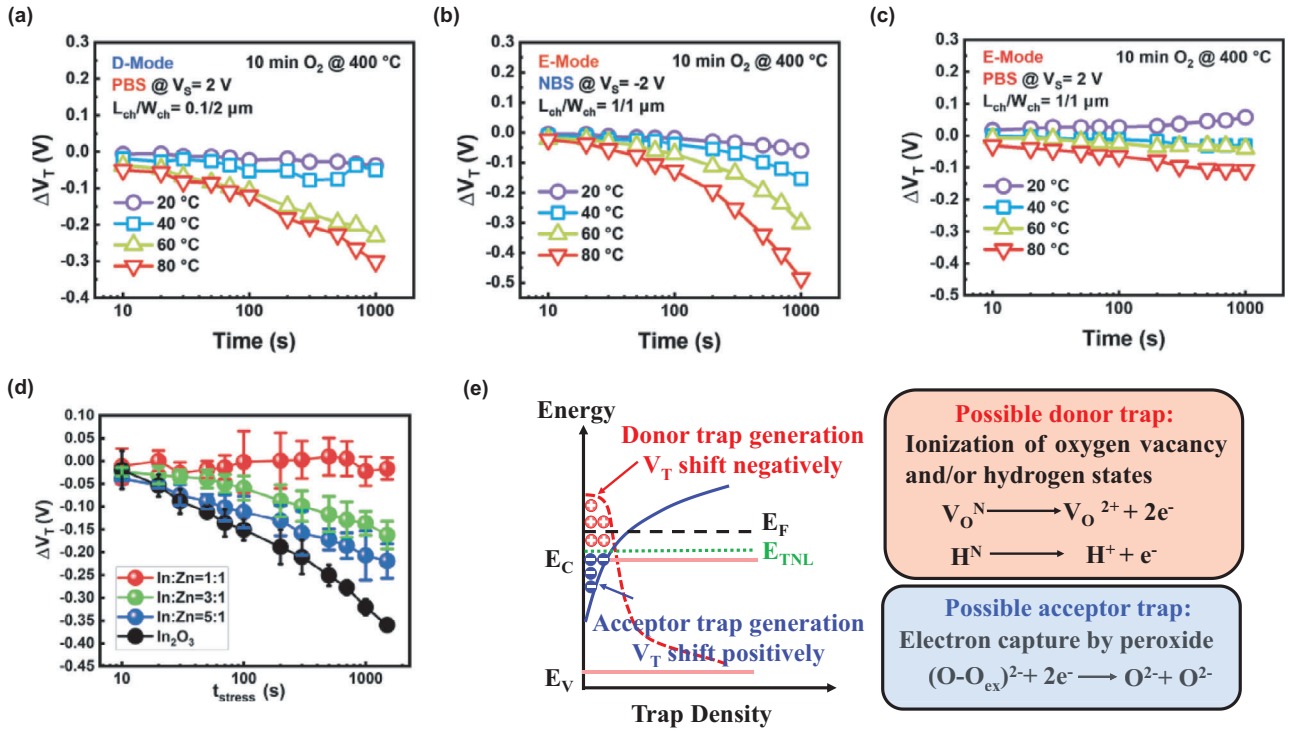

Figure 9. Time evolution of ΔV_T of a) D-mode In_2O_3 FETs under PBS stress of 2 V, b) E-mode In_2O_3 FETs under NBS stress of −2 V, and c) E-mode In_2O_3 FETs under PBS stress of 2 V at different temperatures. d) Time evolution of ΔV_T of InZnO FETs with different In/Zn ratios. e) Models of V_T shifts under BTI test for oxide semiconductor transistors and possible origins of two different types of traps. The PBS measurements here are conducted by DC-IV method.

a wide distribution of trapping time constants, which results in the logarithmic time dependence of BTI that is observed.

Indium oxide transistors exhibit complex BTI behavior, but typically with a small magnitude. In general, the threshold voltage shift does not have a simple one-component fit suggesting competition between multiple mechanisms rather than one dominant trapping type. In some cases, positive bias temperature instability (PBTI) measurements show an anomalous negative V_T shift,[128–130] as shown in **Figure 9**a–c, especially at high temperatures. Finally, the dominant behavior appears to differ significantly depending on the device structure and whether the transistor operates in enhancement or depletion mode. Several techniques have been explored for reducing BTI drift. The remainder of this section will summarize the results to date, comparing with traditional silicon as well as other oxide semiconductors. It will be shown that with the correct design, it is possible to have a very stable high-performance indium oxide device comparable with mature silicon.

5.1. Experimental Results

Since indium oxide and related materials are exclusively n-type, positive bias stress is generally more important for the operation of the devices. In logic circuit operation, the gate of the n-type transistor swings between the positive supply voltage (V_{DD}) and ground. As the most widely studied oxide semiconductor, the PBTI behavior of IGZO devices is most understood. It is common to fabricate amorphous oxide FETs in a buried-gate TFT geometry, in which most of the channel region is exposed to the ambient environment. Strong PBTI shifts have been widely attributed to chemical interactions of oxygen or water with this exposed surface, which can be addressed by encapsulating the channel with an appropriate passivation layer.[127]

Chen et al. investigated PBTI in enhancement-mode indium oxide devices and applied a three-component model to explain the complex behavior.[79,105,107,109,129,137]

$$\Delta V_T\ (t) = A_{it}\, t^n + B_{tr} \log\left(\frac{t}{\tau_{tr}}\right) - C_{dt}\left(1 - e^{-\left(\frac{t}{\tau_{dt}}\right)^{\beta}}\right) \quad (3)$$

in which the terms represent interface trap generation, electron trapping, and donor trap formation, respectively. The model in Equation (3) fits the measured data well for the enhancement-mode devices studied, however, it curiously does not fit nearly identical depletion-mode devices which are studied in ref. [131]. This may be because the dominant bias instability mechanism can depend strongly on the location of the Fermi level in the semiconductor channel.

Ref. [131] also examines encapsulation by a thin layer of ALD-grown HfO_2 to protect the channel from the surrounding environment. This is found to be somewhat successful at reducing the long-term positive bias V_T shift magnitude, but with significant room for further improvement. The initial encapsulation scheme slightly degrades the device SS and adds a static V_T shift (perhaps by oxygen scavenging from the indium oxide layer). A

Table 1. Device studies for reducing BTI shifts.

Approach		NBI behavior	PBI behavior	Ref.
Encapsulation	ALD HfO_2	Slightly worse	Moderate long-term improvement	[131]
	PECVD SiO_2	Moderate improvement	No improvement	[94]
Plasma treatment	CF_4/N_2O	Very large improvement	Large improvement	[132]
Annealing	O_2	Large improvement	Large improvement	[130]
Device geometry	Dual-gate (IWO)	Large improvement	–	[135]
	Gate-all-around	–	–	[115]
Cation doping	IGO	Moderate improvement	Very large improvement	[133]
	IZO	–	Very large improvement	[134]
	IAZO	Some shift present	Stable	[105]
	IGZO	–	Large improvement	[136]

PECVD SiO_2 passivation layer was investigated in comparable indium oxide devices, finding a moderate NBTI improvement but no improvements to the PBTI behavior,[94] Investigation of other encapsulation materials and different deposition schemes may offer a powerful tool to improve the device stability.

In addition to the electrical performance enhancements discussed in Section 4, treatment by plasma or annealing offers an additional potential route to improve the BTI performance of these devices but remains largely unstudied. In one study on the ALD-grown ultra-thin devices, exposure to a weak CF_4/N_2O plasma reduced the room-temperature bias stress V_T shift under 2000 s of bias stress at a +2 V gate bias to −30 mV (compared to −540 mV for an identical device from the same process without plasma treatment).[132] The CF_4/N_2O plasma study noted sizeable improvement to the room-temperature NBI V_T behavior when subject to 2000 s of −4 V gate bias, finding a moderate shift of +150 mV when treated compared to +560 mV when untreated.[132] Plasma and annealing are promising because they have been repeatedly demonstrated to enhance device DC performance (Section 4), and are inexpensive, rapid, and do not add significant processing complexity. Since these treatments are understood to passivate defects, it is obvious why they should also be beneficial for bias instability performance.

As previously discussed, the incorporation of additional cations to grow ternary oxides has also been found to be beneficial for BTI behavior, with the trend continuing in the ultra-thin ALD oxides. The downside discussed in Section 1 applies—namely the mobility is reduced. Indium gallium oxide (IGO) TFTs fabricated in a similar process without further treatment show excellent room-temperature PBI resilience with just a −45 mV shift over 2000 s of stress at a logic-relevant +1 V gate bias.[133] Indium zinc oxide (IZO) TFTs with a 1:1 In:Zn stoichiometric ratio have been shown to offer exceptionally good PBI resistance, with essentially zero V_T shift measured after 1500 s of +3 V gate stress, repeatable across many devices,[134] as shown in Figure 9d.

To explain the above BTI degradation, we propose a model based on the alignment of the CNL in In_2O_3 or doped-In_2O_3 materials and to explain the experiments by using donor-like and acceptor-like trap generation. It is believed that the generation of different types of traps in addition to electron (de)trapping could be the underlying mechanism. Under PBTI stress, a negative V_T shift occurs due to the generation of donor-like traps, especially at high temperatures and D-mode. The donor-like traps may originate from the ionized oxygen vacancy and/or hydrogen state while the acceptor-like traps may be due to the peroxide state with excessive oxygen. By balancing different mechanisms, high bias stability could be achieved.

Table 1 summarizes the literature results for the various approaches to solving BTI issues. Direct numerical comparison between different treatments is not provided as it is difficult to accurately assess. Small differences in BTI measurement technique, such as the delay between stress and measure segments or the type of measurement (full transfer curve, pulsed-mode, etc.) can significantly impact the absolute V_T shift, in addition to subtle process differences which may affect the initial distribution of interface and dielectric traps, but are not easily reported. In lieu of this, a short assessment is provided about the reported effectiveness of each proposed treatment.

It is ultimately a question of process optimization to meet the requirements of a given application. Ultra-thin indium oxide devices without further treatments have already been demonstrated with very low BTI shifts, on a level comparable to mature silicon with logic-relevant ±1 V gate biases applied.[131] The cited work achieved a total V_T shift of just −27.5 mV over 3000 s of +1 V gate bias stress.

6. Summary

In summary, the history leading to the re-emergence of indium oxide, its fundamental material properties, growth techniques with a focus on ALD, the state-of-the-art in device research, and the bias stability of the devices were reviewed. Indium oxide devices have been demonstrated with superior performance to other AOSs and BEOL-compatible semiconductor candidates, largely made possible by the thickness engineering enabled by ALD. The material properties, electron transport in devices, and degradation mechanisms can be understood and unified by incorporating a CNL alignment model with conventional semiconductor material and device physics. The ALD approach to indium oxide and doped indium oxides has demonstrated its potential to yield high-performance semiconductor devices fabricated under BEOL conditions.

Despite the promising performance, a few potential downsides must be acknowledged and considered. Most critically, there is no

possibility of p-type indium oxide devices and as such no possibility for native CMOS logic or bipolar devices. Since the killer feature of indium oxide is its ability to be integrated into the back end of line, this may be acceptable. A suitable BEOL p-type material with good transport properties may also be developed in the future, allowing for more expanded applications. Indium is scarce on Earth and expensive, however, the high-performance devices demonstrated need only nanometers of material at a time, which relaxes the real cost of manufacturing. Finally, indium compounds are known to be toxic to humans but this is manageable with appropriate engineering controls.

In addition to BEOL devices, ALD indium oxide and doped indium oxides can be potential alternative solutions for channel materials for TFTs in display technology. Conventional oxide TFTs manufactured by sputtering suffer from device-to-device variation and reliability issues, and therefore complex internal/external compensation must be used. ALD oxide semiconductors have excellent uniformity by nature due to the layer-by-layer chemical process, so we believe they are very promising alternative new materials for the display industry. On the other hand, considering the superior performance, ALD oxide semiconductor transistors are also promising BEOL-compatible channel materials for monolithic 3D applications. Considering the low off-state leakage current due to the wide bandgap, a monolithic 3D DRAM by ALD oxide semiconductors may become one of the killer applications. Meanwhile, ALD oxide semiconductors provide new opportunities on devices with 3D structures, such as 3D NAND and vertical transistors, fully taking advantage of the conformality of the ALD process. Indium oxide with ultra-high charge density also positions itself as a perfect channel material for ferroelectric field-effect transistors as an emerging memory device for in-memory computing applications. Significant improvement in retention and endurance can be realized due to excellent charge match between the oxide semiconductor channel and the ferroelectric film.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Keywords

amorphous, atomic layer deposition, back-end-of-line, In_2O_3, oxide semiconductors

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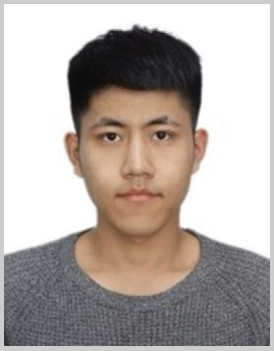

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